

DOCKET NO. FIS9-2003-0186-US1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Dureseti Chidambarao, et al.

Group Art Unit: Unknown

Serial No.: Not assigned yet

Examiner: unknown

Filed: Concurrently herewith

For : IMPROVED NFETs USING GATE INDUCED STRESS MODULATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT
UNDER 37 C.F.R. 1.56**

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the documents listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application.

This citation does not constitute an admission that the cited references are relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. They are merely cited as constituting related art of which the applicant is aware.

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It is respectfully requested that these documents be considered by the Examiner and formally made of record in this application.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Andrew M. Calderon", with a stylized, looping flourish extending to the right.

Andrew M. Calderon

Reg. No. 38,093

Telephone: (703)712-5426

McGuireWoods LLP
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McLean, VA 22102
(703)712-5000

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|---|--|--------------------------|
| FORM PTO-1449 (Modified) | ATTY. DOCKET NO. FIS920030186US1 | SERIAL NO. Unassigned |
| LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT | APPLICANT: Dureseti Chidambarao, et al. | |
| (Use several sheets if necessary) | FILING DATE: Concurrently Herewith | GROUP: Unassigned |

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

| EXAMINER INITIALS | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE (IF APPRO.) |
|----------------------|--------------------|-----------|----------------|-------|----------|----------------------------|
| | 6,228,694 B1 | 5/8/2001 | Doyle et al. | | | |
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FOREIGN PATENT DOCUMENTS

| DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION | |
|--------------------|------|---------|-------|----------|-------------|----|
| | | | | | YES | NO |

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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| | Kern Rim, et al., "Transconductance Enhancement in Deep Submicron Strained-Si <i>n</i> -MOSFETs", International Electron Devices Meeting, 26, 8, 1, IEEE, September 1998. |
| | Kern Rim, et al., "Characteristics and Device Design of Sub-100 nm Strained Si N- and PMOSFETs", 2002 Symposium On VLSI Technology Digest of Technical Papers, IEEE, pp 98-99. |
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| | F. Ootsuka, et al., "A Highly Dense, High-Performance 130nm node CMOS Technology for Large Scale System-on-a-Chip Application", International Electron Devices Meeting, 23.5.1, IEEE, April 2000. |
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| | A. Shimizu, et al., "Local Mechanical-Stress Control (LMC): A New Technique for CMOS-Performance Enhancement", International Electron Devices Meeting, IEEE, March 2001. |
| | K. Ota, et al., "Novel Locally Strained Channel Technique for high Performance 55nm CMOS", International Electron Devices Meeting, 2.2.1, IEEE, February 2002. |

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